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October 5, 2006

The Honorable Joseph J. Farnan, Jr.
United States District Court
For the District of Delaware
844 King Street
Wilmington, DE 19801

ATLANTA
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WASHINGTON, DC

Re: Power Integrations, Inc. v. Fairchild Semiconductor International
USDC-D. Del. - C.A. No. 04-1371 JJF
Response to Fairchild's Request for Claim Interpretation

Your Honor:

Power Integrations respectfully submits its letter brief in response to Fairchild's October 4, 2006 Request for Claim Interpretation ("Fairchild Request") (D.I. 403). In reality, Fairchild's Request is a motion for reconsideration of the Court's claim construction rulings for the '075 Patent (D.I. 232). Simply put, the Court already has decided the construction issues that Fairchild now raises. Knowing that it could not meet the reconsideration standard, Fairchild has recast its Request as seeking constructions for allegedly unconstrued terms. The terms need not and should not be re-construed, and the Court should deny Fairchild's Request.

(1) Standard for Reconsideration of the Court's Markman Order

Fairchild "must show that at least one of the following criteria applies: (1) a change in the controlling law; (2) availability of new evidence not available when the Court made its decision; or (3) need to correct a clear error of law or fact or to prevent manifest injustice," to prevail on its motion for reconsideration. *Lucent Technologies, Inc. v. Extreme Networks, Inc.*, 231 F.R.D. 453, 455 (D. Del. 2005) (internal quotations and citations omitted). "As a general rule, motions for reconsideration should be granted sparingly." *Id.* (internal quotations and citations omitted). Fairchild has not shown a change in law, new evidence, or clear legal error in the Court's Markman Order, because it cannot.

(2) The Terms Already Have Been Construed

The Court already has construed the claim terms Fairchild now submits: "MOS transistor" and "within the substrate."[1] The Court construed these terms to have their plain and ordinary meaning. *See Memorandum and Order* at 9 (D.I. 231) (noting that the Court was adopting what the parties agreed upon). These constructions are:

- **"MOS transistor"** means "a metal-oxide-semiconductor transistor." *Order* at 1.
- **"Substrate"** means "the physical material on which a transistor or microcircuit is fabricated." *Id.*

Fairchild is correct that the Court left open the issues of equivalence and estoppel "until such time as the DMOS issue is properly before the Court."[2] However, now is not that time. As the Court and Fairchild know, Power Integrations is asserting only literal infringement of the '075 Patent – no doctrine of equivalents. Thus, equivalence and estoppel issues are moot. *See Fromson v. Advance Offset Plate, Inc.*, 720 F.2d 1565, 1571 (Fed. Cir. 1983) (finding that if there is literal infringement the doctrine of prosecution history estoppel is "irrelevant").[3]

(3) There Was No Clear Disavowal - DMOS is Not a Limitation

Fairchild now seeks to have the constructions for "MOS transistor" and "substrate" re-construed so as to include a DMOS limitation. However, the Court already has found that DMOS is not a claim term, should not be imported into the claims, and does not limit the literal scope of the claims. *Memorandum and Order* at 7-10 (D.I. 231). Construing the claims to include a DMOS limitation would be wrong now, as it was before.

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[1] Fairchild now seeks to have the phrase "within a substrate" construed. However, the Court already has construed "substrate" and thus decided the issue. "Within" is a plain English word and requires no special construction. *See Research Plastics, Inc. v. Federal Packaging Corp*, 421 F.3d 1290, 1295 (Fed. Cir. 2005) (claim terms are presumed to have the same meaning throughout the claims of a patent).

[2] "Because 'DMOS' is not a claim term, the Court concludes that its meaning is not properly considered in the context of claim construction. Accordingly, the Court declines to provide a construction for the term 'DMOS' in the context of its Markman rulings and will defer construction of this term until such time as the Court is presented with the **equivalence and/or estoppel issues** involving this term." *Memorandum and Order* at 8-9 (emphasis added) (D.I. 231).

[3] Moreover, as the Court noted in its *Markman* ruling [*Memorandum Opinion* at 9 n.1], prosecution history estoppel is a question of law. It is therefore inappropriate for Fairchild to address the estoppel issue to the jury, as it has repeatedly done thus far at trial.

Fairchild claims that Power Integrations disclaimed all DMOS devices when it distinguished the present invention over U.S. Patent No. 4,626, 879 to Colak (hereinafter "Colak"). Power Integrations did not – it disclaimed the type of DMOS device shown in Colak, which is not what Fairchild makes.

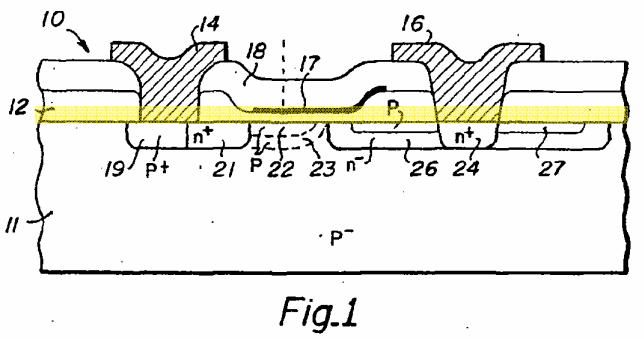

Fig.1

'075 Patent

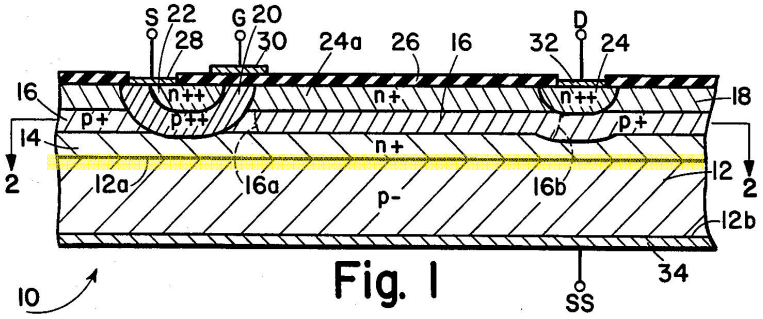

Fig. 1

Colak

Colak discloses a device that has a substrate with three epitaxial layers formed thereon. Colak's doped regions, and in particular its source region 22 and channel 20, are within these epitaxial layers, which are all above the substrate 12. This can be seen clearly in Colak's Figure 1, which shows the substrate as region 12 and the boundary between the substrate and the first epitaxial layer as 12a. Colak explicitly describes surface 12a as the "surface 12a of the substrate." [Colak 3:61] The three layers (14, 16, and 18) containing the doped regions and are all above the substrate.

In contrast, the '075 invention's doped regions, including the source pocket 21 and channel region 22 and 23, are within the substrate 11. These doped regions are diffused into the substrate like water is into a sponge – they are not on top. ['075 Patent at 2:43-46 ("Beneath the source contact 14, a pocket 19 of p+ material and a pocket 21 of n+ material are diffused into the p- substrate 11.")] The surface of the substrate is the yellow highlighted line of Figure 1 of the '075 Patent, above.

Since the substantive distinctions are clear,[4] Fairchild improperly focuses on portions of the file history out of context to try to broaden the statements disclaiming Colak to all DMOS.

> Claim 19 also provides for a pair of laterally spaced source and drain contact pockets within the substrate as is customary for conventional

[4] There are other fundamental differences as well, which the applicant pointed out to the PTO. For example, Colak admittedly does not have the combination of the fifth and sixth elements of claim 1 of the '075 (*i.e.*, the "extended drain region" and "surface adjoining layer" limitations). [PX 8, Amd. After Final, p. 2-3, PIF00056-57]

> MOS transistors and is thus, distinguished from DMOS devices which require a higher threshold voltage.

[DX 201 (Amd (4/7/88), p.6].

> Claim 19 further provides for a substrate having a surface, an insulating layer on the surface of the substrate covering at least that portion between the source contact pocket and the nearest surface-adjoining position of the extended drain region, and a gate electrode on the insulating layer electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjoining position of the extended drain region. Thus, claim 19 is limited to a MOS or MOSFET structure, while Colak shows a D-MOS device.

[DX 102 (Amd after Final (8/12/1988)), p. 3].

These statements refer to the specific Colak device. For example, the first passage distinguishes between the pockets being within the substrate as compared to above the substrate like Colak. Fairchild's proposed construction would mean that the pockets of the preferred embodiments (as shown, for example, in Figures 2, 3, and 5 of the '075 Patent, which all show source pockets (36, 72) within doped regions of the substrate) would be above the substrate – yet this is in direct contradiction to how those embodiments are described in the '075 Patent, and how the '075 Patent was distinguished over Colak.

For the last passage, Fairchild focuses on the last sentence while ignoring all that precedes it. These prior sentences describe the pockets in the '075 as being within the substrate instead of on top of the substrate like Colak. It is this distinction over Colak that Power Integrations disclaimed, nothing more. *See Omega Engineering, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1325-26 (Fed. Cir. 2003) (finding that there must be clear and unmistakable disavowal of claim scope for disclaimer to attach).

Fairchild cites the *Spring Windows* decision in support of its position, but, this case is not relevant here. *Spring Windows Fashion LP v. Now Indus., L.P.*, 323 F.3d 989, 995 (Fed. Cir. 2003). In *Spring Windows*, the patentee argued that a mistake was made by the prosecuting attorney that should be ignored. That is not the case here.

Fairchild also relies heavily on irrelevant evidence in arguing for its constructions. Specifically, Fairchild points to the testimony of inventor Mr. Klas Eklund and the expert testimony of Dr. Gwozdz. This is classic extrinsic evidence that should not be given any weight. *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1584-85

(Fed. Cir. 1996). Further, what, if anything, Fairchild believed or relied on is totally irrelevant to how the claims should be construed.

(a) "MOS transistor"

The Court construed "MOS transistor" to mean "a metal-oxide-semiconductor transistor." Fairchild now seeks to change the construction to "a metal-oxide-semiconductor transistor which excludes DMOS devices," again arguing that Power Integrations disclaimed DMOS. As shown above, there was no such disclaimer. MOS does not exclude DMOS; to the contrary, its undisputed that DMOS is a specific type of MOS. Indeed, the specification explicitly says that the invention could be embodied in a MOS or DMOS structure. ['075 at 3:6-9] Moreover, the term MOS is in the preamble, which does not generally serve to limit the claims and does not do so here. *See Intertool, Ltd. v. Texar Corp*., 369 F.3d 1289, 1295 (Fed. Cir. 2004). The required structure is fully described in the body of the claim.

(b) "Within the substrate"

The Court construed **"**substrate**"** to mean "the physical material on which a transistor or microcircuit is fabricated." *Order* at 1 (D.I. 232). This is also the definition provided by Power Integrations in the prosecution history, which appears in the patent at column 4, lines 55-57. [PX 8, Amd., p. 1, PIF00040] Fairchild tries to import the DMOS limitation to this phrase by redefining the substrate to carve out of the substrate "subsequently doped regions." Specifically, Fairchild now adds "and not within subsequently doped regions" to the Court's previous substrate construction. As shown above, there is no basis for this qualification, particularly given that the applicant provided the definition of "substrate," which the Court adopted, in the very amendment in which the applicant also made the primary statement on which Fairchild relies in constructing its "DMOS disclaimer" argument. *Id.* at p. 1, 6.

(4) Fairchild's Motion for Reconsideration Should be Denied

The Court should not reconsider its constructions, which were properly decided the first time after extensive briefing and arguments by the parties. The lack of an infringement defense is not a justification for this end run on the Court's constructions.

Respectfully,

/s/ William J. Marsden, Jr.

William J. Marsden, Jr.

WJM/kxk

cc: Steven J. Balick, Esq. (By Email)
Bas de Blank, Esq. (By Email)